A METHOD OF FABRICATING A FLASH MEMORY DEVICE

ABSTRACT OF THE DISCLOSURE

A method of fabricating a flash memory device includes forming a device isolation layer at a predetermined region of a semiconductor substrate having a cell array region and a peripheral circuit region. The device isolation layer defines a first active region and a second active region in the cell array region and the peripheral circuit region, respectively. A gate conductive layer is formed on the entire surface of the semiconductor substrate having the device isolation layer. The gate conductive layer is patterned to form a floating gate pattern covering the first active region. At this time, the peripheral circuit region is still covered with the gate conductive layer. An inter-gate dielectric layer and a control gate conductive layer are formed on the entire surface of the substrate including the floating gate pattern. The control gate conductive layer and the inter-gate dielectric layer, which are located in the peripheral circuit region, are selectively removed to expose the gate conductive layer in the peripheral circuit region.